1. (Original) A system-on-a-chip integrated circuit structure comprising:

a bridge having a plurality of channels;

a processor local bus connected to said bridge, wherein said bridge includes a first channel dedicated to said processor local bus;

at least one logic device connected to said processor local bus;

a peripheral device bus connected to said bridge, wherein said bridge includes a second channel dedicated to said peripheral device bus;

at least one peripheral device connected to said peripheral device bus;

at least one memory unit connected to said bridge, wherein said bridge includes a third channel dedicated to said memory unit; and

at least one input/output unit connected to said bridge, wherein said bridge includes a fourth channel dedicated to said input/output unit.

2. (Original) The structure in claim 1, wherein each of said channels includes buffer memories adapted to store data when a previous data transfer is being performed.

3. (Original) The structure in claim 2, wherein said buffer memories comprise first-in first-out buffer memories.

4. (Original) The structure in claim 1, wherein each of said channels includes a multi- port static random access memory (SRAM) adapted to store data when a previous data transfer is being performed.

5. (Original) The structure in claim 1, wherein each of said channels includes a multiplexor adapted to selectively connect to other channels.

6. (Original) The structure in claim 1, wherein said at least one memory unit comprises a first-type memory unit and a second-type memory unit different than said

first- type memory unit, wherein said third channel is dedicated to said first-type memory unit and said bridge includes a fifth channel dedicated to said second- type memory unit.

7. (Original) The structure in claim 6, wherein said first-type memory unit comprises static random access memory (SRAM) and said second-type memory unit comprises synchronous dynamic random access memory (SDRAM).

8. (Original) The structure in claim 1, wherein said at least one input/output unit comprises one or more of a peripheral interface, graphics interface, and serial bus interface, and wherein said bridge includes dedicated channels for each of said peripheral interface, graphics interface, and serial bus interface.

9. (Original) The structure in claim 1, wherein said at least one peripheral device includes one or more of a serial connection, network interface connection, and programmable input/output connection each connected to said peripheral device bus.

10. (Original) A system-on-a-chip integrated circuit structure comprising:

a bridge having a plurality of channels;

at least one bus connected to a unique dedicated channel in said bridge;

at least one memory unit connected to a unique dedicated channel in said bridge; and

at least one input/output unit connected to a unique dedicated channel in said bridge.

11. (Original) The structure in claim 10, wherein said at least one bus includes:

a processor local bus connected to said bridge, wherein said bridge includes a first channel dedicated to said processor local bus; and

a peripheral device bus connected to said bridge, wherein said bridge includes a second channel dedicated to said peripheral device bus,

wherein said structure further comprises:

at least one logic device connected to said processor local bus; and

at least one peripheral device connected to said peripheral device bus.

12. (Original) The structure in claim 10, wherein each of said channels includes buffer memories adapted to store data when a previous data transfer is being performed.

13. (Original) The structure in claim 12, wherein said buffer memories comprise first-in first-out buffer memories.

14. (Original) The structure in claim 10, wherein each of said channels includes a multi- port static random access memory (SRAM) adapted to store data when a previous data transfer is being performed.

15. (Original) The structure in claim 10, wherein each of said channels includes a multiplexor adapted to selectively connect to other channels.

16. (Original) The structure in claim 10, wherein said at least one memory unit comprises a first-type memory unit and a second-type memory unit different than said first-type memory unit, wherein said bridge includes a first channel is dedicated to said first-type memory unit and a second channel dedicated to said second-type memory unit.

17. (Original) The structure in claim 16, wherein said first-type memory unit comprises static random access memory (SRAM) and said second-type memory unit comprises synchronous dynamic random access memory (SDRAM).

18. (Original) The structure in claim 10, wherein said at least one input/output unit comprises one or more of a peripheral interface, graphics interface, and serial bus interface, and wherein said bridge includes unique dedicated channels for each of said peripheral interface, graphics interface, and serial bus interface.

19. (Original) The structure in claim 11, wherein said at least one peripheral device includes one or more of a serial connection, network interface connection, and programmable input/output connection each connected to said peripheral device bus.

20. (Original) A bridge for a system-on-a-chip (SoC) integrated circuit structure comprising:

a plurality of dedicated channels each uniquely connected to one or more of:

at least one bus within said SoC;

at least one memory unit within said SoC;

at least one input/output unit within said SoC; and

at least one peripheral device within said SoC.

21. (Original) The structure in claim 20, wherein said at least one bus includes:

a processor local bus connected to said bridge, wherein said bridge includes a first channel dedicated to said processor local bus; and

a peripheral device bus connected to said bridge, wherein said bridge includes a second channel dedicated to said peripheral device bus,

wherein said SoC includes:

at least one logic device connected to said processor local bus; and

at least one peripheral device connected to said peripheral device bus.

22. (Original) The structure in claim 20, wherein each of said channels includes buffer memories adapted to store data when a previous data transfer is being performed.

23. (Original) The structure in claim 22, wherein said buffer memories comprise first-in first-out buffer memories.

24. (Original) The structure in claim 20, wherein each of said channels includes a multi- port static random access memory (SRAM) adapted to store data when a previous data transfer is being performed.

25. (Original) The structure in claim 20, wherein each of said channels includes a multiplexor adapted to selectively connect to other channels.

26. (Original) The structure in claim 20, wherein said at least one memory unit comprises a first-type memory unit and a second-type memory unit different than said first-type memory unit, wherein said bridge includes a first channel is dedicated to said first-type memory unit and a second channel dedicated to said second-type memory unit.

27. (Original) The structure in claim 26, wherein said first-type memory unit comprises static random access memory (SRAM) and said second-type memory unit comprises synchronous dynamic random access memory (SDRAM).

28. (Original) The structure in claim 20, wherein said at least one input/output unit comprises one or more of a peripheral interface, graphics interface, and serial bus interface, and wherein said bridge includes unique dedicated channels for each of said peripheral interface, graphics interface, and serial bus interface.

29. (Original) The structure in claim 21, wherein said at least one peripheral device includes one or more of a serial connection, network interface connection, and programmable input/output connection each connected to said peripheral device bus.